CBCS SCHEME

USN | | | | | | | | | | |

15NT34

# Third Semester B.E. Degree Examination, June/July 2018

## MOSFETS and Digital Circuits

Time: 3 hrs. Max. Marks: 80

**Note: Answer any FIVE full questions, choosing one full question from each module.**



### Module-1

1 a. With the help of output characteristics (or) V-I curves discuss four regions of operation of JFET? Mention typical valves of gate to source voltage, drain to source voltage and drain current on the V-I curves. **(06 Marks)**

b. With the help of neat sketches discuss SOI fabrication process of MOS transistor. Mention the advantages of SOI process with regard to N-well process. **(06 Marks)**

c. Define the following: Channel length modulation and body effect. **(04 Marks)**

**OR**

2 a. Draw the internal structure and VI curves for n-channel and p-channel FET. Discuss in detail working principle of n-channel JFET. **(06 Marks)**

b. With the help of neat sketches discuss the operation of MOSFET and mention the three regions of operation. Discuss the input and output characteristics of MOS transistor. **(06 Marks)**

c. Define Melay and Moore machines. **(04 Marks)**

### Module-2

3 a. Write the small signal model for nmos transistor operating in saturation region and mention the IDS expression. **(08 Marks)**

b. An input periodic pulse of duration 10ns with on time duration of 4ns and voltage excursions between 0v to 3v in applied at the input of cmos inverter. The rise time and fall time of input signal is 0.2ns and 0.4ns. Plot the output signal of cmos inverter. **(04 Marks)**

c. In a medicine processing unit, it is required to keep track of number of bottle being filled. A digital circuit is required to keep track of the number of bottles being filled and inform the manager after every 10 bottles are filled. What kind of Digital circuit is recommended for this purpose? **(04 Marks)**

**OR**

4 a. It is required to analyze the transfer characteristics of cmos inverter. Use appropriate graph to discuss the operating regions of cmos inverter. Mention the most preferred regions of operation of cmos inverter. **(06 Marks)**

b. Draw the cmos circuit schematic of 2 input NAND gate and 3 inputs NOR gate. Illustrate the working of 2 input NAND gate and verify its truth table. **(04 Marks)**

c. Mention two types of scaling in MOSFET and discuss in detail advantages and disadvantages of scaling. In the power expression $P = CV^2f$ if the voltage is scaled by a factor S, how is the power being affected? **(06 Marks)**

### Module-3

5 a. Realize the expression $Q^+ = CIK\ D + \overline{CIK}\ Q$ using cmos transmission gate. **(06 Marks)**

b. Discuss second order effects in mos transistors. **(04 Marks)**

c. Discuss the working principle of ring oscillator. It is required to generate two clock signals that are complementary to each other. How can the ring oscillator used for this purpose? Can the ring oscillator be also used to generate clock signal with phase delays. Draw neat sketches to discuss. **(06 Marks)**

**OR**

6 a. It is required to drive a digital circuit using both positive level and negative level latch. Construct the positive and negative level sensitive latch using 2:1 multiplexers and cmos inverters. Draw the cmos circuit and discuss the working principle using timing diagrams. **(08 Marks)**

b. Define setup time, hold time and clock to q delay using appropriate timing diagrams. **(04 Marks)**

c. Draw the cmos circuit for 2 input XOR gate. **(04 Marks)**

## Module-4

7 a. Mention the various parasitic capacitance in mos transistor using internal structure of mos transistor. **(04 Marks)**

b. With the help of truth table discuss the working principle of Johnson counter and mention its applications. **(04 Marks)**

c. With the help of neat diagram, discuss the working of Serial In Serial Out shift register. Illustrate the data loading operation in SISO to load data of 1101 and also illustrate how this loaded data 1101 is read out serially. **(08 Marks)**

**OR**

8 a. Draw the digital circuit diagram of 4-bit Parallel In Serial Out shift register. Illustrate the working of PISO shift register with example. **(08 Marks)**

b. Realize 2 input XNOR gate using cmos circuits. **(04 Marks)**

c. Describe the operation of 3-bit synchronous binary counter with timing diagram [Hint : Use JK flip-flop] **(04 Marks)**

## Module-5

9 a. For the transition table in table 9(a) draw FSM diagram.

| Transition Table | | |
|---|---|---|
| Present state | Next state | |
| | X = 0 | X = 1 |
| A | A, 0 | B, 1 |
| B | A, 0 | C, 0 |
| C | C, 0 | D, 0 |
| D | A, 0 | E, 1 |
| E | A, 1 | E, 0 |

Table 9(a) **(08 Marks)**

b. A digital circuit is required to generate clock signals of 8MHz and 16MHz. The input clock to the digital circuit is 64MHz. Design the circuit and discusses its operation using timing diagrams. **(08 Marks)**

**OR**

10 a. Write the transition table and FSM diagram for a 3-bit up/down counter. **(06 Marks)**

b. For the transition table given in Table Q 10(b). Write the FSM diagram using Moore machine.

| Transition Table | | |
|---|---|---|
| Present state | Next state, output (y) | |
| | X = 0 | X = 1 |
| A | A, 0 | B, 0 |
| B | A, 0 | C , 0 |
| C | C, 0 | D, 0 |
| D | A, 0 | E, 1 |
| E | A, 0 | B, 0 |

Table Q10(b) **06 Marks**

c. Realize 2:1 multiplexer using cmos transmission gate. **(04 Marks)**

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